08-21-00 A

PTO/SB/05 (2/98)

Type a plus sign (+) inside this box [+]

UTILITY PATENT APPLICATION TRANSMITTAL

(for nonprovisional applications under 37 CFR § 1.53(b))

Attorney Docket No.	500644.01
First Inventor or Application Identifier	Brent Keeth
Title	METHOD AND SYSTEM FOR USING DYNAMIC RANDOM ACCESS MEMORY AS CACHE MEMORY
Express Mail Label No.	EL476400619US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Box Patent Application, Assistant Commissioner for Patents, Washington, D.C. 20231

1. [ ] General Authorization Form & Fee Transmittal *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [Total Pages] 15 *(preferred arrangement set forth below)*
   - Descriptive Title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [Total Sheets] 2
4. Oath or Declaration [Total Pages]
   a. [ ] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
5. [ ] Incorporation By Reference *(useable if box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer-Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copy of IDS Citation
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [X] Other: Certificate of Express Mail

17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information below and in a preliminary amendment*

[ ] Continuation [ ] Divisional [ ] Continuation-In-Part (CIP) of prior Application No.: _____ Filed _____

Prior application information: Examiner _____ *Group / Art Unit* _____

[ ] Claims the benefit of Provisional Application No. _____

CORRESPONDENCE ADDRESS

Edward W. Bulchis, Esq.
Dorsey & Whitney LLP
1420 Fifth Avenue, Suite 3400
Seattle, Washington 98101-4010
(206) 903-8800 *phone*
(206) 903-8820 *fax*

Respectfully submitted,

TYPED or PRINTED NAME Edward W. Bulchis REGISTRATION NO. 26,847

SIGNATURE Edward W. Bulchis Date August 17, 2000

o:\ip\documents\clients\micron technology\600\500644.01\500644.01 sb05.doc

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	: Brent Keeth, Charles H. Dennison, Brian M. Shirley and Kevin J. Ryan	Attorney Docket No.: 500644.01
Filed	: August 17, 2000	
Title	: METHOD AND SYSTEM FOR USING DYNAMIC RANDOM ACCESS MEMORY AS CACHE MEMORY	

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

Box Patent Application
Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

I hereby certify that the enclosures listed below are being deposited with the United States Postal Service "EXPRESS MAIL Post Office to Addressee" service under 37 C.F.R. § 1.10, Mailing Label Certificate No. EL476400619US, on August 17, 2000, addressed to Box Patent Application, Assistant Commissioner for Patents, Washington, DC 20231.

Respectfully submitted,

DORSEY & WHITNEY LLP

Juanette West

West Courier

Enclosures:
Postcard
Form PTO/SB/05
Specification, Claims, Abstract (15 pages)
2 Sheets of Drawings (Figures 1-3)
Information Disclosure Statement, Form PTO-1449, and
Cited References (1)

METHOD AND SYSTEM FOR USING DYNAMIC RANDOM ACCESS MEMORY AS CACHE MEMORY

TECHNICAL FIELD

The present invention is directed memory devices, and, more particularly, to a system and method for allowing dynamic random access memory devices to be used as cache memory.

BACKGROUND OF THE INVENTION

Memory devices are used in a wide variety of applications, including computer systems. Computer systems and other electronic devices containing a microprocessor or similar device typically include system memory, which is generally implemented using dynamic random access memory ("DRAM"). The primary advantage of DRAM is that it uses relatively few components to store each bit of data, and is thus relatively inexpensive to provide relatively high capacity system memory. A disadvantage of DRAM, however, is that their memory cells must be periodically refreshed. While a memory cell is being refreshed, read and write accesses to other rows in the memory array are blocked. The need to refresh memory cells does not present a significant problem in most applications, but it can prevent their use in applications where immediate access to memory cells is required or highly desirable.

Also included in many computer systems and other electronic devices is a cache memory. The cache memory stores instructions and/or data (collectively referred to as "data") that is frequently accessed by the processor or similar device, and may be accessed substantially faster than data can be accessed in system memory. It is important for the processor or similar device to be able to access the cache memory as needed. If the cache memory cannot be accessed for a period, the operation of the processor or similar device must be halted during this period. Cache memory is typically implemented using static random access memory ("SRAM") because such memory need not be refreshed and is thus always accessible for a write or a read memory access. However, a significant disadvantage of SRAM is that each memory cell requires a relatively large number of components, thus making SRAM data storage relatively expensive. It would be desirable to implement cache memory using DRAM

because high capacity cache memories could then be provided at relatively little cost. However, a cache memory implemented using DRAMs would be inaccessible at certain times during a refresh of the memory cells in the DRAM. For example, during refresh of a row of memory cells, it would be impossible to read data from or write data to other rows of memory cells. As a result of these problems, DRAMs have not generally been considered acceptable for use as cache memory or for other applications requiring immediate access to memory.

Attempts have been made to use DRAM as cache memory, but these attempts have not been entirely successful in solving the refresh problem so that these prior art devices are not always available for a memory access. These prior art devices have attempted to "hide" memory refreshes by including a small SRAM to store one or more rows of DRAM data during refresh of a row being addressed. However, in practice, there are still some memory access situations in which these prior art devices may not be accessed, thus suspending the operation of a processor or similar device.

There is therefore a need for a DRAM that effectively hides memory refresh under all memory access situations so that the DRAM may provide relatively inexpensive, high capacity cache memory.

SUMMARY OF THE INVENTION

A method of caching data and a cache system that may be used in a computer system includes a DRAM having a plurality of refresh blocks and a pair of SRAMs having a capacity of at least the capacity of the refresh blocks. If a block of the DRAM to which data is attempting to be written is being refreshed, the data is instead written to one of the SRAMs. When the refresh of that block has been completed, the data is transferred from the SRAM to a block of the DRAM to which data was attempted to be written. If a block to which data is attempting to be written is being refreshed and data is being transferred from the one SRAM to a block of the DRAM, the data is instead written to the other SRAM. As a result, there is always one SRAM available into which data may be written if a refresh block to which the write was directed is being refreshed.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a computer system containing a cache memory in accordance with one embodiment of the invention.

Figure 2 is a block diagram of a cache system that may be used as a cache memory in the computer system of Figure 2 in accordance with one embodiment of the invention.

Figure 3, is a diagram conceptually illustrating a DRAM and SRAM arrays shown in the cache system of Figure 2.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 is a block diagram of a computer system 10 that includes a processor 12 for performing various computing functions by executing software to perform specific calculations or tasks. The processor 12 is coupled to a processor bus 14 that normally includes an address bus, a control bus, and a data bus (not separately shown). In addition, the computer system 10 includes a system memory 16, which is typically dynamic random access memory ("DRAM"). As mentioned above, using DRAM at the system memory 16 provides relatively high capacity at relatively little expense. The system memory 16 is coupled to the processor bus 14 by a system controller 20 or similar device, which is also coupled to an expansion bus 22, such as a Peripheral Component Interface ("PCI") bus. A bus 26 coupling the system controller 20 to the system memory 16 also normally includes an address bus, a control bus, and a data bus (not separately shown), although other architectures can be used. For example, the data bus of the system memory 16 may be coupled to the data bus of the processor bus 14, or the system memory 16 may be implemented by a packetized memory (not shown), which normally does not include a separate address bus and control bus.

The computer system 10 also includes one or more input devices 34, such as a keyboard or a mouse, coupled to the processor 12 through the expansion bus 22, the system controller 20, and the processor bus 14. Also typically coupled to the expansion bus 22 are one or more output devices 36, such as a printer or a video terminal. One or more data storage devices 38 are also typically coupled to the expansion bus 22 to allow the processor 12 to store data or retrieve data from internal or external storage media (not shown). Examples of typical storage devices 38 include

hard and floppy disks, tape cassettes, and compact disk read-only memories (CD-ROMs).

The processor 12 is also typically coupled to cache memory 40 through the processor bus 14. In the past, the cache memory 40 was normally implemented using static random access memory ("SRAM") because such memory is relatively fast, and does not require refreshing and may thus always be accessed. However, as explained above, using SRAM for the cache memory 40 is a relatively expensive means for providing a relatively high capacity because of the large number of components making up each SRAM storage cell compared to the number of components in each DRAM storage cell.

According to one embodiment of the invention, the cache memory 40 shown in Figure 1 is implemented using a cache system 50, an example of which is shown in Figure 2. The cache system 50 includes components normally found in a DRAM, including an address decoder 52 receiving addresses through an address bus 53, a row driver circuit 54 adapted to receive row addresses from the address decoder 52, and a column driver circuit 56 adapted to receive column addresses from the address decoder 52. The row driver circuit 54 is coupled to word lines (not shown) in a memory array 60, and the column driver circuit 56 is coupled to digit lines (not shown) in the memory array 60. As shown in Figure 2, the memory array 60 is either physically or logically divided into a plurality of banks 60a-n. Each bank 60a-n is divided into one or more refresh blocks, each containing a plurality of rows that are contemporaneously refreshed. The column driver 56 is also coupled to a sense amplifier/write driver circuit 64 to route write data and read data from and to, respectively, a data input/output buffer 66 through an internal data bus 68. The data input/output buffer 66 is, in turn, coupled to an external data bus 70. As in conventional DRAMs, the cache system 50 also includes a control circuit 72 that includes a command buffer 74 receiving command signals through a command bus 76 and generating appropriate control signals for controlling the operation of the cache system 50. The control circuit 72 also includes a refresh controller 78 for refreshing the DRAM array 60 one refresh block at a time.

Unlike conventional DRAMs, the cache system 50 also includes two SRAM arrays 80, 84 that are each coupled to the sense amplifier/write driver circuit 64

to access data in the DRAM array 60. The SRAM arrays 80, 84 are also coupled to the refresh controller 78. The refresh controller 78 receives addresses from the address decoder 52, and it applies addressing and control signals to the row driver 54.

The operation of the command buffer 74, refresh controller 78 and the SRAM arrays 80, 84 in relation to the other components of the cache system 50 will now be explained with reference to the diagram of Figure 3, which conceptually illustrates the DRAM array 60 and the SRAM arrays 80, 84 shown in Figure 2. As mentioned above, the DRAM array is divided into a plurality of refresh blocks. The refresh blocks may be part of the same or different banks 60a-n of DRAM memory, or physically different DRAM devices. In the embodiment shown in Figure 3, each of the refresh blocks 61a-n has a capacity of Y bits, and each of the SRAM arrays 80, 84 also has a capacity of Y bits. Each of the refresh blocks 61a-n may be individually refreshed under control of the refresh controller 78 (Figure 2). The DRAM array 60 has twice the normal number of input/output ("I/O") lines, which are configured so that two blocks can be simultaneously accessed. As a result, it is possible for data to be read from or written to one refresh block 61a-n of the DRAM array 60 at the same time data are being transferred from one of the SRAM arrays 80, 84 to another block 61a-n of the DRAM array 60.

In operation, a read from a refresh block 61a-n that is not being refreshed is read in a conventional manner. Similarly, a write to a block 61a-n that is not being refreshed is accomplished in a conventional manner. Thus, no problem is presented in either writing to or reading from a refresh block 61a-n that is not being refreshed. In either of these cases, data access to the cache system 50 does not require any wait, thus allowing the cache system 50 to be used as a cache memory in place of a typically used SRAM without any performance limitations.

The potential problem in accessing the cache system 50 is in the event of a read or a write to a refresh block 61a-n being refreshed, and, in particular, to a different row than the row in that block that is being refreshed. The cache system 50, preferably the refresh controller 78, may check each memory command prior to initiating a refresh in a block 61a-n to determine if the memory command is a read. If a read command directed to a block 61a-n that is about to be refreshed is received, then the refresh is not initiated. In this regard, it is assumed that the duration of a refresh is

shorter than the duration of a memory read operation. Each time a read is executed, the read data are written to one of the SRAMs 82, 84. As a result, the read data are subsequently accessible in one of the SRAMs 82, 84, thereby allowing the portion of the block 61a-n that stored such data to be refreshed despite subsequent reads from that that portion. In the case of sequential reads from the rows of a block 61a-n, the reads will refresh the rows.

In the event a memory access is a write to a block 61a-n being refreshed, the write data is instead written to one of the SRAM arrays 80, 84. When the refresh of the block to which the write was directed has been completed, the refresh controller 78 starts a refresh of another block 61a-n of the DRAM array 60. While this subsequent refresh is occurring, the data that had been written to one of the SRAM arrays 80, 84 is transferred to the block 61a-n to which the earlier write was directed. If, during refresh of the second block 61a-n, a read or a write is directed toward that block 61a-n, then that data is instead stored in the other one of the SRAM arrays 80, 84. By the time the refresh of the second block 61a-n has been completed, transfer of the data from first one of the SRAM arrays 80, 84 to the first block 61a-n will have been completed, and that SRAM array 80, 84 will be available to store write data that is subsequently directed to any other block 61a-n that is being refreshed. Therefore, an SRAM array 80, 84 is always available to store write data that is directed to a refresh block 61a-n of the memory array 60 that is being refreshed. As a result, data may always be read from or written to the cache system 50 without the need for to wait for the completion of a refresh of any block 61a-n the cache system 50. The cache system 50 may therefore be used as a cache memory in place of an SRAM that is typically used, thereby providing high capacity caching at relatively little cost.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

1. A cache system comprising:

at least one DRAM array divided into a plurality of blocks;

first and second SRAM arrays each having a capacity at least as large as the capacity of a block of the DRAM array;

an address decoder coupled to receive a memory address and being operable to decode the address and generate decoded address signals corresponding thereto;

an input/output circuit coupled to the DRAM array, the SRAM array, and the address decoder, the input/output circuit being operable to respond to a first control signal by coupling write data from an external data terminal to a location in a block of the DRAM array corresponding to the decoded address signals, or to respond to a second control signal by coupling write data from the external data terminal to a location in the first or second SRAM arrays, or to respond to a third control signal by coupling data from one of the SRAM arrays to a location in a block of the DRAM array corresponding to the decoded address signals; and

a control circuit coupled to the DRAM array, the SRAM array, the address decoder, and the input/output circuit, the control circuit being operable to refresh the DRAM array one block at a time, the control circuit further being operable to generate the first control signal when the block of the DRAM array corresponding to the decoded address signals is not being refreshed, to generate the second control signal when the block of the DRAM array corresponding to the decoded address signals is being refreshed, to generate the third control signal when the block of the DRAM array that was being refreshed when the data was stored in the SRAM array is no longer being refreshed.

2. The cache system of claim 1 wherein the control circuit comprises:

a refresh controller coupled to the DRAM array, the refresh controller being operable to refresh the DRAM array one block at a time; and

a control buffer structured to receive a memory command and to generate the first, second and third control signals corresponding thereto.

3. The cache system of claim 1 wherein the block of DRAM array are physically part of a single DRAM array.

4. The cache system of claim 1 wherein the an input/output circuit comprises a plurality of complimentary input/output line pairs, the input/output lines being sufficient in number that a first pair of input/output lines may be coupled to one block of the DRAM array while a second pair of input/output lines may be coupled to another block of the DRAM array.

5. A cache system comprising:

at least one DRAM array divided into a plurality of blocks;

first and second SRAM arrays each having a capacity at least as large as the capacity of a block of the DRAM array, the SRAM arrays being coupled to the DRAM array for direct transfer of data from either of the SRAM arrays to any block of the DRAM array if the block of the DRAM array is not being refreshed; and

an input/output circuit coupled to the DRAM array and the SRAM array, the input/output circuit being operable to store write data in a block of the DRAM array to which the write data was directed, and to store write data directed to any block of the DRAM array in either of the SRAM arrays if the block to which the write data was directed is being refreshed.

6. The cache system of claim 5 wherein the block of DRAM array are physically part of a single DRAM array.

7. The cache system of claim 5 wherein the an input/output circuit comprises a plurality of complimentary input/output line pairs, the input/output lines being sufficient in number that a first pair of input/output lines may be coupled to one block of the DRAM array while a second pair of input/output lines may be coupled to another block of the DRAM array.

8. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a system controller coupled to the processor bus;

a system memory coupled to the processor through the system controller; and

a cache system coupled to the processor bus, the cache system comprising:

at least one DRAM array divided into a plurality of blocks;

first and second SRAM arrays each having a capacity at least as large as the capacity of a block of the DRAM array;

a data transfer circuit coupled to the DRAM array and the SRAM array, the data transfer circuit being operable to respond to a first control signal by coupling write data to the first or second SRAM arrays, or to respond to a second control signal by coupling data from one of the SRAM arrays to a location in a block of the DRAM; and

a control circuit coupled to the DRAM array and the SRAM array, the control circuit being operable to refresh the DRAM array one block at a time, the control circuit further being operable to generate the first control signal when the block of the DRAM array to which write data is being directed is being refreshed, and to generate the second control signal when the block of the DRAM array that was being refreshed when the data was stored in the SRAM array is no longer being refreshed.

9. The computer system of claim 8 wherein the control circuit comprises:

a refresh controller coupled to the DRAM array, the refresh controller being operable to refresh the DRAM array one block at a time; and

a control buffer structured to receive a memory command and to generate the first, second and third control signals corresponding thereto.

10. The computer system of claim 8 wherein the block of DRAM array are physically part of a single DRAM array.

11. The computer system of claim 8 wherein the an input/output circuit comprises a plurality of complimentary input/output line pairs, the input/output lines being sufficient in number that a first pair of input/output lines may be coupled to one block of the DRAM array while a second pair of input/output lines may be coupled to another block of the DRAM array.

12. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a system controller coupled to the processor bus;

a system memory coupled to the processor through the system controller; and

a cache system coupled to the processor bus, the cache system comprising:

at least one DRAM array divided into a plurality of blocks;

first and second SRAM arrays each having a capacity at least as large as the capacity of a block of the DRAM array;

an input/output circuit coupled to the DRAM array and the SRAM array, the input/output circuit being operable to write data directed to any block of the DRAM array in either of the SRAM arrays if the block to which the write data was directed is being refreshed; and

a control circuit coupled to the DRAM array and the SRAM array, the control circuit being operable to cause either of the SRAM arrays to transfer data stored in the SRAM array to any block of the DRAM array if the block of the DRAM array is no longer being refreshed.

13. The computer system of claim 12 wherein the block of DRAM array are physically part of a single DRAM array.

14. The computer system of claim 12 wherein the an input/output circuit comprises a plurality of complimentary input/output line pairs, the input/output lines being sufficient in number that a first pair of input/output lines may be coupled to one block of the DRAM array while a second pair of input/output lines may be coupled to another block of the DRAM array.

15. A method of caching data, comprising:

providing a DRAM having a plurality of blocks each of which may be refreshed;

providing first and second SRAMs having a capacity of at least the capacity of the DRAM blocks;

addressing a first block of the DRAM in an attempt to write data into the first block of the DRAM;

if the first block of the DRAM is being refreshed during the attempt, writing the data into the first SRAM;

after the first block of the DRAM is no longer being refreshed, transferring data stored in the first SRAM to the first block of the DRAM;

addressing a second block of the DRAM in an attempt to write data into the second block of the DRAM;

if the second block of the DRAM is being refreshed during the attempt, and data is being transferred from the first SRAM to the first block of the DRAM, writing the data into the second SRAM; and

after the second block of the DRAM is no longer being refreshed, transferring data stored in the second SRAM to the second block of the DRAM.

16. The method of claim 15 further comprising writing data into the first SRAM if the second block of the DRAM is being refreshed during the attempt to write the data into the second block and data is not being transferred from the first SRAM to the first block of the DRAM.

17. The method of claim 15 further comprising writing the data into the first of the DRAM if the first block of the DRAM is not being refreshed during the attempt.

18. The method of claim 15 further comprising:

addressing a third block of the DRAM in an attempt to write data into the third block of the DRAM;

if the third block of the DRAM is being refreshed during the attempt, and data is being transferred from the second SRAM to the second block of the DRAM, writing the data into the first SRAM; and

after the third block of the DRAM is no longer being refreshed, transferring data stored in the first SRAM to the third block of the DRAM.

19. The method of claim 15 further comprising:

addressing a first block of the DRAM in an attempt to read data from the first block of the DRAM; and

outputting data from the first block of the DRAM.

20. The method of claim 19 wherein the act of outputting data from the first block of the DRAM is accomplished regardless of whether or not the first block of memory is being refreshed.

21. The method of claim 15 further comprising:

addressing the first block of the DRAM in an attempt to read data from the first block of the DRAM; and

outputting data from the first block of the DRAM; and

caching the data output from the first block of the DRAM in the first SRAM.

22. The method of claim 21 further comprising

addressing the first block of the DRAM in an attempt to read data from the first block of the DRAM; and

outputting data from the first block of the first SRAM.

23. A method of caching data, comprising:

providing a DRAM having a plurality of blocks each of which may be refreshed;

providing first and second SRAMs having a capacity of at least the capacity of the DRAM blocks;

sequentially attempting to write data to blocks of the DRAM;

if a block to which data is attempting to be written is being refreshed, writing the data to one of the SRAMs;

when the refresh of a block has been completed, transferring data from the SRAM to which the data had been written to a block of the DRAM to which data was attempted to be written; and

if a block to which data is attempting to be written is being refreshed and data is being transferred from the one SRAM to a block of the DRAM, writing the data to the other SRAM.

24. The method of claim 23 further comprising, if the block to which data is attempting to be written is not being refreshed, writing the data to the block of the DRAM.

25. The method of claim 23 further comprising:

attempting to read data from a block of the DRAM; and

outputting data from the block of the DRAM to which an attempt to read data is directed.

26. The method of claim 25 wherein the act of outputting data from the block of the DRAM is accomplished regardless of whether or not the block of memory is being refreshed.

27. The method of claim 25 further comprising:

attempting to read data from a block of the DRAM;

outputting data from the block of the DRAM to which an attempt to read data is directed and

caching the data output from the block of the DRAM in one of the SRAMs.

METHOD AND SYSTEM FOR USING DYNAMIC RANDOM ACCESS MEMORY AS CACHE MEMORY

ABSTRACT OF THE DISCLOSURE

A cache memory system and method includes a DRAM having a plurality of banks, each of which may be refreshed under control of a refresh controller. In addition to the usual components of a DRAM, the cache memory system also includes 2 SRAMs each having a capacity that is equal to the capacity of each bank of the DRAM. In operation, data read from a bank of the DRAM are stored in one of the SRAMs so that repeated hits to that bank are cached by reading from the SRAM. In the event of a write to a bank that is being refreshed, the write data are stored in one of the SRAMs. After the refresh of the bank has been completed, the data stored in the SRAM are transferred to the DRAM bank. A subsequent read or write to a second DRAM bank undergoing refresh and occurring during the transfer of data from an SRAM to the DRAM is stored in the second bank. If, however, the second bank is being refreshed, the data are stored in the other SRAM. By the time data have been stored in the SRAM, the SRAM previously used to store write data has transferred the data to the first DRAM bank and in thus available to store a subsequent write. Therefore, an SRAM bank is always available to store write data in the event the DRAM bank to which the data are directed is being refreshed.

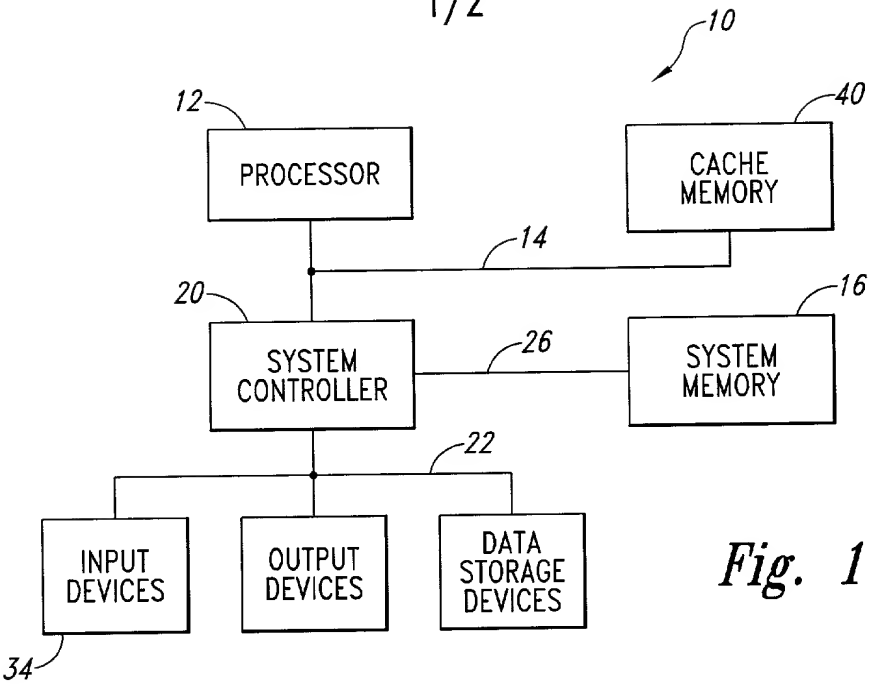
10
12
PROCESSOR
40
CACHE MEMORY
14
20
SYSTEM CONTROLLER
26
16
SYSTEM MEMORY
22
INPUT DEVICES
OUTPUT DEVICES
DATA STORAGE DEVICES
34

Fig. 1

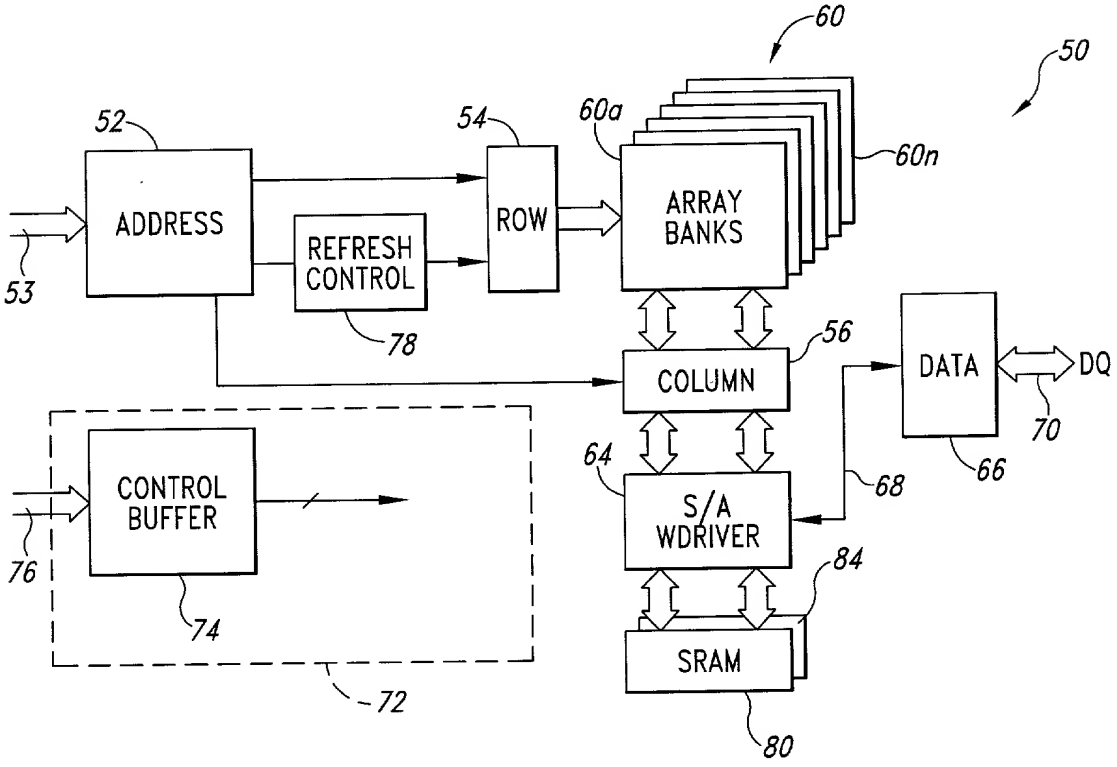
60
50
52
54
60a
60n
ADDRESS
ROW
ARRAY BANKS
53
REFRESH CONTROL
78
56
COLUMN
DATA
DQ
70
66
64
68
CONTROL BUFFER
S/A WDRIVER
84
76
74
SRAM
72
80

Fig. 2

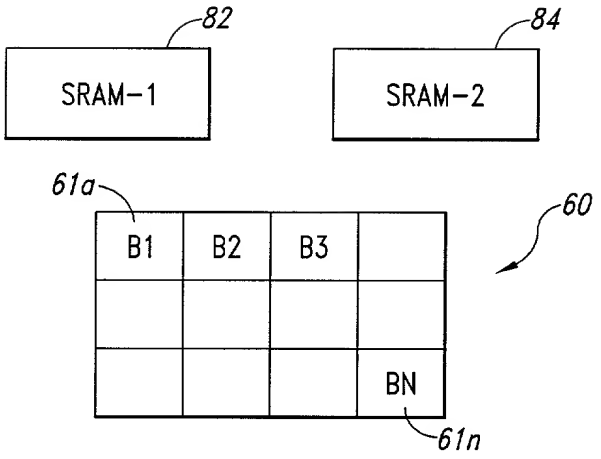

Fig. 3